Design of PD-PWM Based Asymmetrical 15-Level Reduced Switch Multilevel Inverter for PV Applications

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ABSTRACT: This paper presents a new single-phase, 15-level inverter for solar photovoltaic (PV) applications. It features fewer components and can be used to extract more energy from the modules. The proposed inverter can help improve system efficiency and lower costs.The proposed converter can be used to boost the output voltage of the solar PV modules from the MPPT to the maximum level. It is tested using the dSPACERTI 1104 controller and the software packages Simulink and MATLAB. The results of the study demonstrate that the proposed device can perform well under different load conditions.

key words: Solar photovoltaic(PV) inverter, MPPT, converter, total harmonic distortion (THD).

1.INTRODUCTION

Because of the vast usage of the fossil fuels, there is a sharp decrement in the availability of fossil fuel resources. To meet the day-to-day requirements of electricity, it's time to shift to the renewable energy sources. With the advancements in solar energy, the control techniques of grid connected inverters has been deploying from the few years. In order to obtain the above mentioned features , a multilevel inverter with minimum number of switches can be implemented to get a smooth sine wave . MLI's is widely used in high power applications such as large induction drive , UPS systems and FACTS systems.

Required output will be obtained from several level of dc links that are used in the circuit .Most commonly there are three different types of multilevel inverter topologies [1]-[2] used and they are Diode-clamped MLI's, Flying capacitor MLI's and Cascaded H-Bridge MLI's. Basically, three control techniques are available for controlling the grid connected multilevel inverters and those are Carrier wave comparison technique, Hysteresis loop control technique and predictive control technique. The widely used technique is the carrier wave comparison control, which tracks the output current by using a PI Controller [3]. But, it fails in reducing the steady-state error between the target current and the original current. The simplest control technique is the hysteresis loop control technique and it has the advantage of having good robustness [4]-[6], but it has high ripple content in the output current, which may increase the losses and thereby reducing the efficiency of the system. The another major drawback is the unstable switching frequency. Model Predictive control is the main branch of Predictive control techniques. A model has to be established for the system in MPC [7]-[12]. Depending upon the designed model, the upcoming values of the variables can be predicted. Based on the comparison of the predicted values and the required reference values, the control action at this present moment will be taken. MPC structure is very simple for designing and modelling. Predictive control mode can be implemented on a digital signal processor and its output has small distortions in the current and harmonics are minimized.

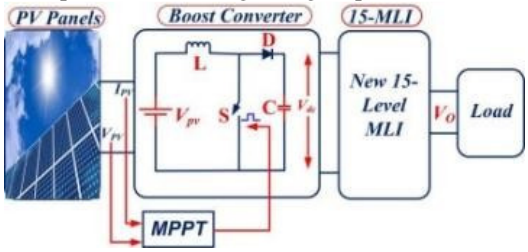

FIGURE 1. Proposed system configuration.

1.CONFIGURATION OF PROPOSED SYSTEMS

Figure 1 depicts the proposed Solar PV Arrays-based converter boost converter with an integrated inverter. Cascaded or parallel photovoltaic cells must be connected based on whether higher voltage or current is required. They are built to last and can withstand the harshest environmental conditions. This Solar PV cell design is accomplished by simulating natural environmental conditions, which are then processed to produce the Irradiance vs Time graph and the Temperature vs Time graph, both of which have been simulated for ten seconds. A solar cell can be represented as a current source connected in parallel to a diode, with the output of the current source being directly proportional to the amount of light falling on the cell. The diode thus defines the VI characteristics of the cell. It cannot use this model to simulate reality because it lacks other external factors besides sunlight. These, however, can be solved by increasing complexity and accuracy. The diodes are then connected in parallel with two distinct sets of saturation current. Consider the temperature dependence of the diode and its saturation current connected with a series of resistances in this programme.

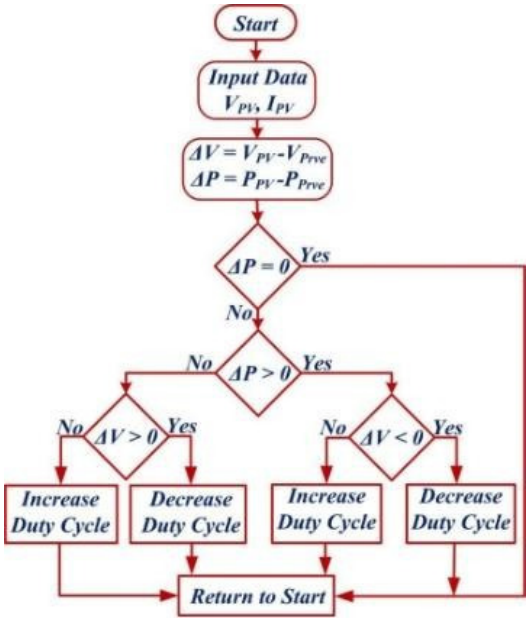

FIGURE 2. MPPT flow chart.

The quality of the output of a power-producing device is determined by its ability match the curve. This is because, unlike other facilities, renewable sources can't be easily controlled. They have various external factors that can affect the output, which is why algorithms are developed to ensure that the power supply is always regulated. This case involves the implementation of a modified version of the algorithm known as the maximum power point tracking. This electronic boost converter is used in combination with a solar cell array to provide the best possible power output. This model was chosen to study the scope of work and the various aspects of a project in the context of the development of a tracking algorithm for real-time radiation therapy. It takes into account the various peak power points of the system and compares them to the strategies and configurations that can be used to achieve the best possible results. The conventional DC to DC converter is necessary because the voltage generated by renewable sources is extremely low and difficult to regulate. As a result, these converters assist the system in reaching the required voltage level for long-term practical operation. C and L are the names given to the capacitor and inductor with values of 3.2nF and 94.22uH, respectively.

TABLE 1. System variables.

Item	Parameters
VPV	115V
Vo	400V
fs	100kHz
Capacitor	3.2nF
Inductor	94.22Uh
Duty ratio	71.25%
IGBT	CM75DU-12, 600V, 75A
dSPACE RTI Controller	1104

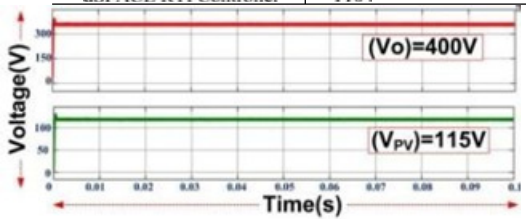

FIGURE 3. Converter and solar PV output waveforms from simulation.

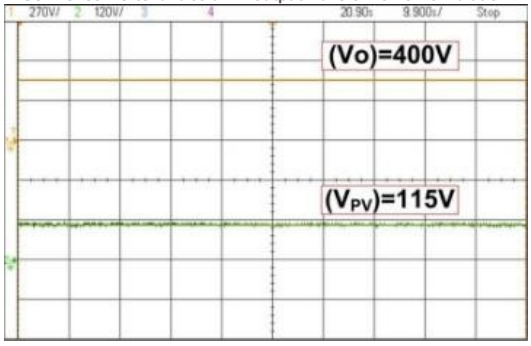

FIGURE 4. Converter and solar PV output waveforms were examined.

It acts as a gate pulse to the boost converter, which adds a delay to the system's maximum power point tracker. To measure the current and voltage of the device, set up an ammeter and a voltmeter. Then, boost the converter and a snubber circuit, which has a resistance of 100, by setting the capacitor's maximum and infinite values. After 0.019 seconds, the boost voltage of the converter, which is 400 volts, is generated.

$$Vo = \frac{Vpv}{(1-D)} \quad (1)$$

The sources for the proposed system are taken into account by the PV simulator 5kW & 8A. The converter simulation and experimental results are displayed in Figures 3–4 for solar PV. Increased DC-linking voltage from solar PV is possible with the boost converter. The obtained DC-link voltage can be fed into the proposed inverter, which will generate an AC stepped waveform.

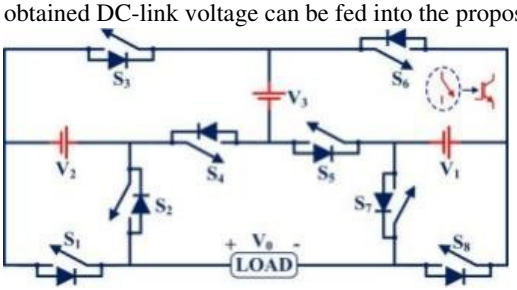

FIGURE 5. Proposed topology of 15 levels.

TABLE 2. Switching states for 15L-MLI

1	S2, S3, S5, S7
2	S2, S3, S5, S8
3	S1, S3, S7, S5
4	S1, S3, S5, S8
5	S2, S3, S6, S7
6	S2, S3, S6, S8
7	S1, S3, S6, S7
8	S2, S4, S5, S7
9	S2, S4, S5, S8
10	S1, S4, S5, S7
11	S1, S4, S5, S8
12	S2, S4, S6, S7
13	S2, S4, S6, S8
14	S1, S4, S6, S7
15	S1, S4, S6, S8

1. PROPOSED 15-LEVEL MLI

A new 15-level inverter shown in Figure 5 is based on a boost converter's DC-link voltage. It features eight switches and three DC-sources. The design of the proposed inverter takes into account the strategy of keeping short circuits out of the path of current. The initial level can be achieved by switching the switches S2, 3, S5, S7, and S8 in a closed path. The total voltage of the system is calculated by taking into account the blocking voltage of the switches. In the second mode, the switches S8, S2, and S3 are conduction. These are chosen to avoid short circuits, and even the sum of the lower the blocking voltages of a semiconductor switch, the lower its cost-effectiveness and the TSV. Table 1 shows the selection patterns of switches up to 15 levels, and these are chosen based on the conditions. The overall loop of the switch conduction helps in reducing the voltage across the switches and improving the efficiency of an inverter.

In order to generate 15 levels of output voltage, an inverter is proposed with asymmetrical DC input sources in a 1:2:5 ratio. Source voltages are taken as Vdc = V1 = 57.15V, V2 = 114.3V, and V3 = 285.75V, respectively, as shown in Table 2. Gate pulses are generated using the staircase PWM technique. In mode 1, the number of V2 + V3 switches that are ON while the other switches are OFF determines the output voltage.

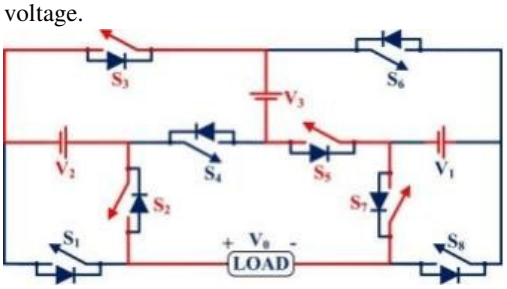

FIGURE 6. Case-1 for the 15MLI

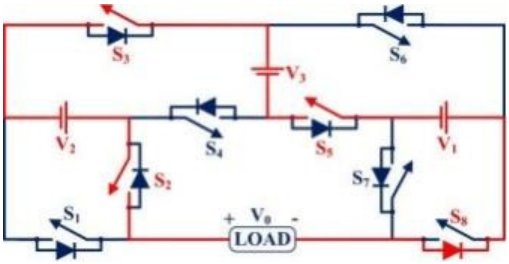

FIGURE 7. Case-2 for the 15MLI.

The output voltage in mode-2 is V1 + V2 + V3, the S2, S3, S5, S8, and S9 switches are ON, and the remaining switches are OFF. In mode-3, the S1, S3, S7, and S5 switches are ON, while the remaining switches are OFF, and the output voltage is V3. In mode-4, the output voltage is the number of V1 + V3, the S1, S3, S5, and S8 switches are turned on, and the remaining switches are turned off. In mode-5, the output voltage equals V1 + V2, the S2, S3, S6, S7 switches are turned on, and the remaining switches are turned off. The output voltage of the S2 and S3 switches is equal to V2. The other switches are turned on and off. In mode 6, the output voltage of the S6 and S8 switches is equal to V2. In mode 7, the output voltage of the S1 and S3 switches is equal to V1. The remaining switches are also turned on. In mode 8, the output voltage of the S2 and S4 switches is ON, while the other switches are off. The S2, S4, S5, S8 and other switches are ON in mode 9, while the others are off. In mode 10, the S1, S4, S5, S7 and other switches are ON, while the others are off. In mode 11, the S1, S4, S5, S8 and other switches are ON, while the others are off. The output voltage is - (-V1 + V3) in mode-12, with the S2, S4, S6, S7 switches ON and the remaining switches OFF. In mode-13, the S2, S4, S6, S8, and S10 switches will be ON, while the remaining switches will be OFF; the output voltage is -V3. The output voltage is - (-V1+V2+V3) in mode-14, with the S1, S4, S6, S7 switches ON and the remaining switches OFF. In mode-15, the S1, S4, S6, and S8 switches are turned on, while the remaining switches are turned off, and the output voltage is - (V2 + V3). All operational modes are depicted in Fig.6 to Fig.21 based on the conduction of switches and the expected waveform.

A. *CIRCUIT PARAMETERS DESIGN*

The oversimplified questionnaires below can be used to calculate the suggested inverter circuit parameters, such as the number of levels (NL), number of switches (NSW), number of DC sources (NSDC), and peak output voltage (VOP).

$$NSDC = n \quad (2)$$

$$NSW = (2nk1+1) + (2nk2+1) + \ldots\ldots\ldots + (2nkj+1) \quad (3)$$

$$NL = (2nk1+1-1)+(2nk2+1-1) \ldots + (2nkj+1-1) \quad (4)$$

$$VOP = ((2nk1+1-2)/2+(2nk2+1-2)/2 + \ldots\ldots + (2nkj+1-2)/2) \times Vdc \quad (5)$$

Where n and k represent the proposed inverter's sources and modules, respectively. Equations (2), (3), (4), and (5) are solved for the parameters with n=3 and

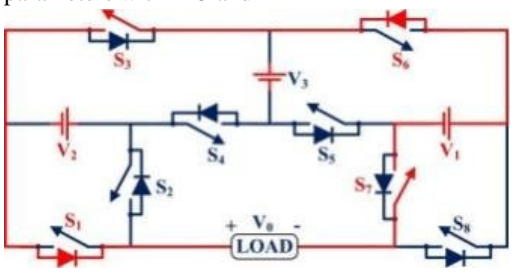

FIGURE 12. Case-7 for the 15MLI.

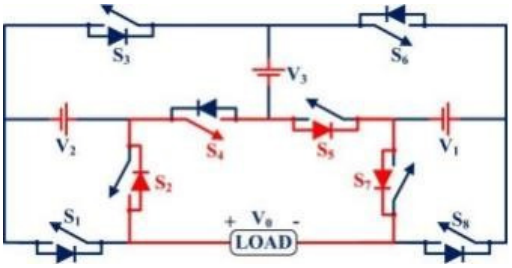

FIGURE 13. Casee-8 for the 15MLI.

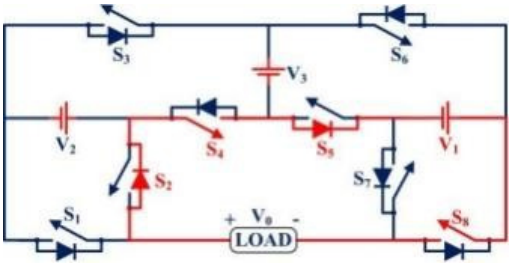

FIGURE 14. Case-9 for the 15MLI.

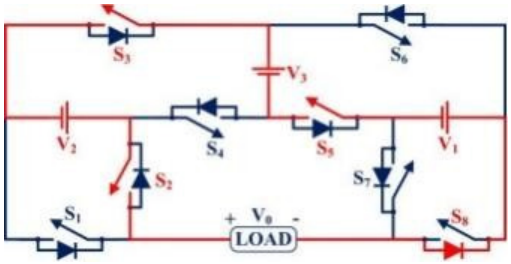

FIGURE 15. Case-10 for the 15MLI.

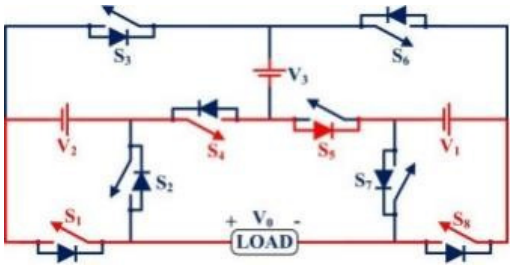

FIGURE 16. Case-11 for the 15MLI.

k=1 and $V_{dc} = V_1 = 57.15V$, respectively. The $N_{SDC} = 3$, $N_{SW} = (2^{3+1}) = 8$, $N_L = (2^{3+1} - 1) = 15$, and

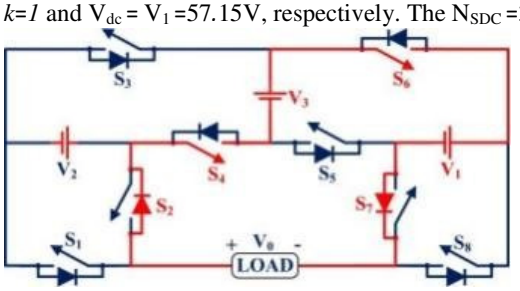

FIGURE 17. Case-12 for the 15MLI.

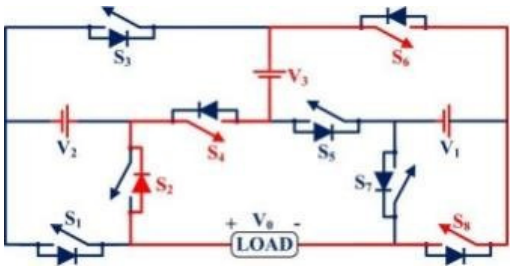

FIGURE 18. Case-13 for the 15MLI.

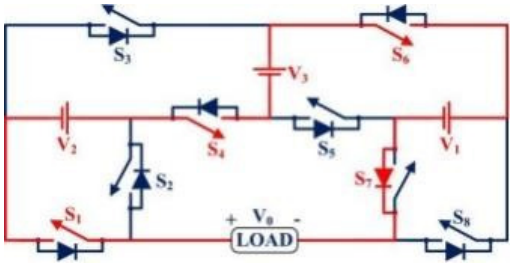

FIGURE 19. Casee-14 for the 15MLI.

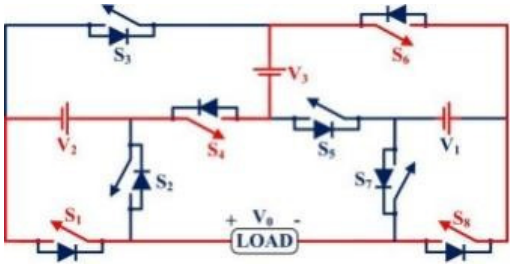

FIGURE 20. Casee-15 for the 15MLI.

$V_{OP} = \left(\frac{2^{3+1}-2}{2}\right) * 57.15 = 400.$05V. The proposed inverter was implemented using two basic modules (k=2) to generate a 29-output voltage level.

B. RESULTS ANALYSIS

Using MATLAB/Simulink simulation and the dSPACE RTI11014 Controller for experimental validation, the suggested inverter was verified as shown in Fig. 34. The output waveforms and THD of the simulation are displayed in Figures 22–27. The high power CM75DU-

12H IGBTs with 600V & 75A ranges are used for the experiment, along with the PV simulator 5kW & 8A sources. The dSPACE controller generates gate pulses by employing the TLP250 driver technique of the staircase PWM.

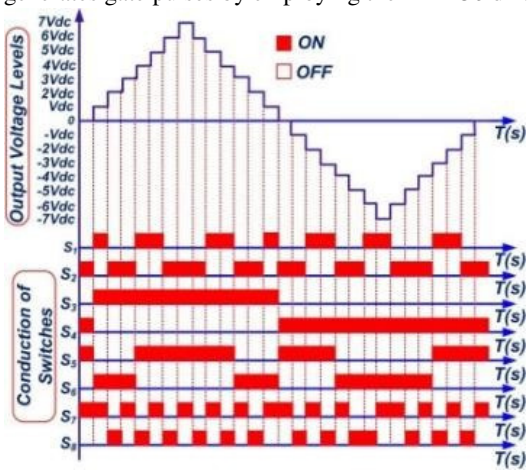

FIGURE 21. The predicted 15MLI waveform.

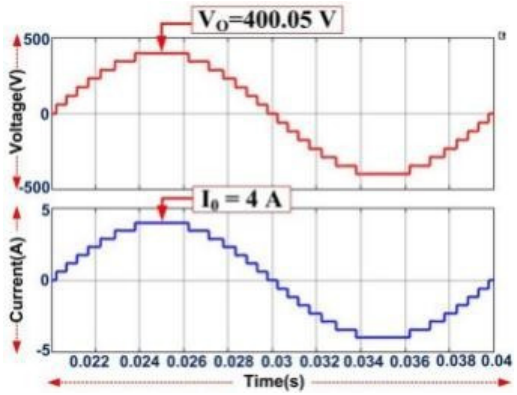

FIGURE 22. The 15MLI's single-cycle output waveform.

Single-phase loads with a resistance of 100 ohms, 175 mh, and 0.5 HP and a power factor of 0.75 were utilized for the simulation and experiment, respectively. The source voltages used are Vdc = V1 = 57.15V, V2 = 114.3V, and V3 = 285.75V in order to obtain the maximum peak output voltage Vo=400.05V. The robustness of the proposed 15-level inverter is analysed with linear and non-linear loads.

As per Figs. 28 and 29, the experimentally obtained output power, output voltage, and output current for the proposed inverter with linear loads are Po=782.55W, Vo=400.05V, Io=4A, Vrms=277.5V, and Irms=2.82A. In Fig. 30, the inverter's performance and effectiveness are confirmed with a motor load (non-linear) using the output voltage and current (Vo=400.05V, Io=6.5A). The dynamic load is used to test and incorporate swaps from linear to nonlinear. The suggested inverter achieves the maximum system peak output voltage of 400V and keeps a stable output during dynamic load changes, as shown in Figs. 31 and 32. According to IEEE standards, the efficiency is 95.237%, and the experimental THD is 4.41%. To enhance power quality, the proposed inverter can be linked to the grid and FACTS.

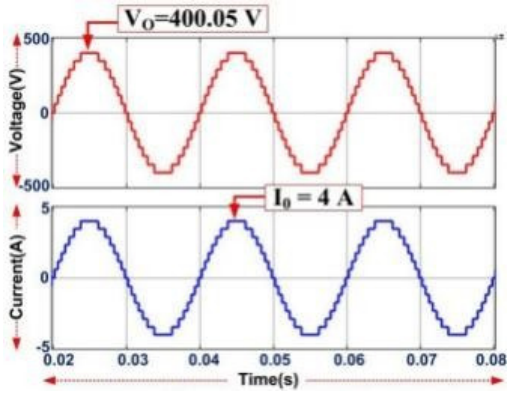

FIGURE 23: The 15MLI's two-cycle output waveform.

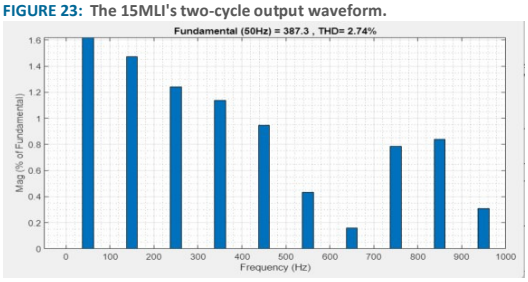

FIGURE 24. The 15MLI THD simulation.

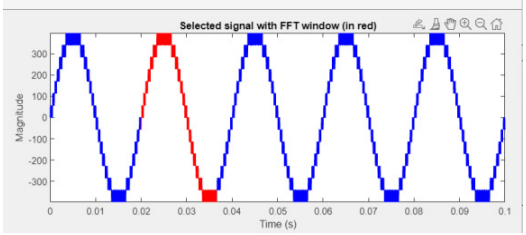

FIGURE 25. Waveform of the 15MLI experiment

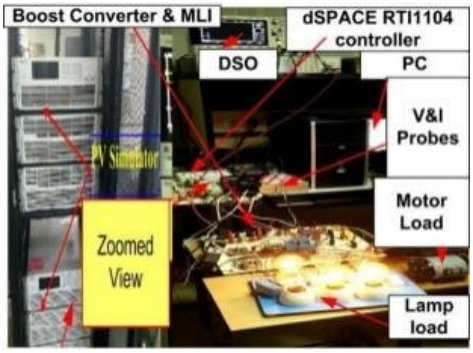

FIGURE 26. Prototype model of 15MLI.

TABLE 3. Levels vs Modulation index.

MI (Modulation Index)	L (Number of Levels)
0.14	3
0.29	5
0.43	7
0.57	9
0.71	11
0.86	13
1.00	15

FIGURE 27. Levels vs MI of 15MLI.

1. CONCLUSION

This paper proposes a new type of 15-level inverter for use in solar PV systems. It uses a boost converter to generate an AC output voltage. The proposed inverter has fewer components and low total harmonic distortion .A proposed inverter uses eight insulated-gating bipolar transistors, which are triggered by a pulse-width measurement technique known as the staircase modulation technique. It has high efficiency, lower losses, and low harmonic distortion. Compared to multilevel models, this design offers significant reduction in complexity and stress. The design of the proposed inverter was tested with different types of load conditions, such as non-linear and linear loads. It was able to maintain stable performance under dynamic conditions, which makes it suitable for applications.

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